ROC920030113US1

In the Claims:

Please amend claims 1, 7, 11-13 and 15-19 such that the pending claims read as follows:

Claim 1 (currently amended): A method of selecting a signal from a plurality of signals comprising:

providing a plurality of multiplexers, each multiplexer ~~adapted~~ configured to selectively output one of a plurality of input signals input by the multiplexer using an output of the multiplexer;

selecting an input signal from one of the plurality of multiplexers to output;

outputting the selected input signal from the output of the one of the plurality of multiplexers;

forcing the outputs of the other of the plurality of multiplexers to a predetermined logic state; and

combining the outputs of the plurality of multiplexers so as to output the selected input signal.

Claim 2 (original): The method of claim 1 wherein selecting the input signal from one of the plurality of multiplexers to output includes:

generating a plurality of select signals; and

providing a unique portion of the select signals to each of the plurality of multiplexers.

Claim 3 (original): The method of claim 2 wherein generating the plurality of select signals includes

generating select signals, wherein only one of the select signals is of a high logic state.

Claim 4 (original): The method of claim 1 wherein forcing the outputs of the other of the plurality of multiplexers to a predetermined logic state includes:

generating a plurality of activation signals to activate one of a pull-up circuit and a pull-down circuit in the other of the plurality of multiplexers; and

forcing the outputs of the other of the plurality of multiplexers to the predetermined logic state using the one of the pull-up circuit and the pull-down circuit.

Claim 5 (original): The method of claim 1 wherein outputting the selected input signal from the output of the one of the plurality of multiplexers, and forcing the outputs of the other of the plurality of multiplexers to a predetermined logic state are performed in parallel.

Claim 6 (original): The method of claim 1 wherein combining the outputs of the plurality of multiplexers comprises employing one of a logic OR and a logic AND operation to combine the outputs of the plurality of multiplexers.

Claim 7 (currently amended): A multiplexer circuit ~~adapted~~ configured to select a signal from a plurality of signals comprising:

a plurality of multiplexers, each multiplexer ~~adapted~~ configured to selectively output one of a plurality of signals input by the multiplexer using an output of the multiplexer;

a first decoder circuit coupled to the plurality of multiplexers and ~~adapted~~ configured to generate a plurality of select signals to select an input signal from one of the plurality of multiplexers to output;

a second decoder circuit coupled to the plurality of multiplexers and ~~adapted~~ configured to generate a plurality of activation signals to force the outputs of the other of the plurality of multiplexers to a predetermined logic state; and

a logic circuit coupled to the plurality of multiplexers and ~~adapted~~ configured to combine the outputs of the plurality of multiplexers so as to output the selected input signal.

Claim 8 (original): The multiplexer circuit of claim 7 wherein each of the plurality of activation signals correspond to a different one of the plurality of multiplexers.

Claim 9 (original): The multiplexer circuit of claim 7 wherein the first and second decoder circuits employ a common input to generate the plurality of select signals and the plurality of activation signals.

Claim 10 (original): The multiplexer circuit of claim 7 wherein the first and second decoder circuits operate in parallel.

Claim 11 (currently amended): The multiplexer circuit of claim 7 wherein the logic circuit is ~~adapted~~ configured to perform an AND operation on the outputs of the plurality of multiplexers.

Claim 12 (currently amended): The multiplexer circuit of claim 7 wherein the logic circuit is ~~adapted~~ configured to perform an OR operation on the outputs of the plurality of multiplexers.

Claim 13 (currently amended): The multiplexer circuit of claim 7 wherein the first decoder circuit is further ~~adapted~~ configured to output a unique portion of the select signals to each of the plurality of multiplexers.

Claim 14 (original): The multiplexer circuit of claim 13 wherein the plurality of select signals and the plurality of input signals input by each of the plurality of multiplexers have an equal number.

Claim 15 (currently amended): The multiplexer circuit of claim 7 wherein the first decoder circuit is further ~~adapted~~ configured to generate a plurality of select signals, wherein only one of the plurality of select signals is of a high logic state.

Claim 16 (currently amended): The multiplexer circuit of claim 7 wherein each of the plurality of multiplexers includes a pull-up circuit; and

wherein the second decoder circuit is further ~~adapted~~ configured to:

generate a plurality of activation signals to activate the pull-up circuits coupled to the other of the plurality of multiplexers; and

force the outputs of the other of the plurality of multiplexers to the predetermined logic state

using the pull-up circuits coupled to the other of the plurality of multiplexers.

Claim 17 (currently amended): The multiplexer circuit of claim 16 wherein the logic circuit is ~~adapted~~ configured to perform an AND operation on the outputs of the plurality of multiplexers.

Claim 18 (currently amended): The multiplexer circuit of claim 7 wherein each of the plurality of multiplexers includes a pull-down circuit; and

wherein the second decoder circuit is further ~~adapted~~ configured to:

generate a plurality of activation signals to activate the pull-down circuits coupled to the other of the plurality of multiplexers; and

force the outputs of the other of the plurality of multiplexers to the predetermined logic state using the pull-down circuits coupled to the other of the plurality of multiplexers.

Claim 19 (currently amended): The multiplexer circuit of claim 18 wherein the logic circuit is ~~adapted~~ configured to perform an OR operation on the outputs of the plurality of multiplexers.